IN THE CLAIMS:

Please amend claims 1, 5, 6, 11, 13, 15, 17, 20, 30, 32, 34, 36, 37, 39, 40 and 42 and cancel claims 25, 26, 28, 29, 31, 33 and 35 as follows:

Claim 1 (currently amended): A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a plurality of first internal ~~circuit~~ circuits on the insulating substrate, the first semiconductor chip having a plurality of first terminal ~~pad connecting to~~ pads, each of which is connected to one of the first internal ~~circuit~~ circuits and a plurality of conductive relay [[pad]] pads, each of which is isolated from the first terminal [[pad]] pads, and each of the conductive relay [[pad]] pads including a first area and a second area, which is different from the first area, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of first metal [[bump]] bumps, each of which is formed on one of the conductive relay [[pad]] pads in the first area;

a second metal bump formed on the second terminal pad;

a first bonding wire, wherein one end thereof is formed on one of the first terminal [[pad]] pads and the other end is formed on the first conductive pattern;

a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of the first metal bump on one of the conductive relay [[pad]] pads in the first area; and

a third bonding wire, wherein one end thereof is formed on the one of the conductive relay [[pad]] pads in the second area and the other end is formed at the top of the second metal bump[[;]] ,

wherein the lengths of the first, second and third bonding wire are

approximately the same.

Claim 2 (original): A multi-chip package type semiconductor device, as claimed in claim 1, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 3 (cancelled).

Claim 4 (cancelled).

Claim 5 (currently amended): A multi-chip package type semiconductor device, as claimed in claim [3] 2, wherein <u>each of</u> the conductive relay [[pad]] <u>pads</u> is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same

as that from the side of the first semiconductor chip to the second area.

Claim 6 (currently amended): A multi-chip package type semiconductor device, as claimed in claim [3] 2, wherein one of the conductive relay relay [[pad]] pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 7 (original): A multi-chip package type semiconductor device, as claimed in claim 6, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claims 8-10 (cancelled).

Claim 11 (currently amended): A multi-chip package type semiconductor

device, as claimed in claim [3] 2, wherein the first metal bump is spaced apart from ~~the first bond~~ the one end of the third bonding wire, but is electrically connected to ~~the first bond~~ the one end of the third bonding wire via the conductive relay pad.

Claim 12 (cancelled).

Claim 13 (currently amended): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a plurality of first terminal [[pad]] pads and a plurality of conductive relay [[pad,]] pads, each of the conductive relay [[pad]] pads including a first area and a second area, which is different from the first area, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a second terminal pad, connected to one of the conductive relay [[pad]] pads in the second area;

a plurality of first metal [[bump]] bumps, each of which is formed on one of the conductive relay [[pad]] pads in the first area;

a second metal bump formed on the second terminal pad;

a first internal terminal connected to one of the first terminal [[pad]] pads;

a second internal terminal connected to one of the conductive relay [[pad]] pads in the first area;

a first bonding wire, wherein one end thereof is formed on the first internal terminal and the other end is formed on one of the first terminal [[pad]] pads;

a second bonding wire, wherein one end thereof is formed on the second internal terminal and the other end is formed at the top of the first metal bump formed on one of the conductive relay pads; and

a third bonding wire, wherein one end thereof is formed on the one of the conductive relay [[pad]] pads in the second area and the other end is formed at

the top of the second metal bump.

Claim 14 (original): A multi-chip package type semiconductor device, as claimed in claim 13, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 15 (currently amended): A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor chip having a plurality of first internal ~~circuit~~ circuits, a plurality of first terminal ~~pad connecting to~~ pads, each of which is connected to one of the first internal ~~circuit~~ circuits and a plurality of conductive relay [[pad]] pads, each of which is isolated from the first terminal [[pad]] pads, wherein each first

terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of first metal [[bump]] bumps, each of which is formed on one of the conductive relay [[pad]] pads;

a second metal bump formed on the second terminal pad;

a first bonding wire, wherein one end thereof is formed on one of the first terminal [[pad]] pads and the other end is formed on the first conductive pattern;

a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of one of the first metal [[bump]] bumps; and

a third bonding wire, wherein one end thereof is formed at the top of the one of the first metal [[bump]] bumps and the other end is formed at the top of the second metal bump;

wherein the lengths of the first, second and third bonding wire are

approximately the same.

Claim 16 (original): A multi-chip package type semiconductor device, as claimed in claim 15, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

Claim 17 (currently amended): A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor chip having a plurality of first internal ~~circuit~~ circuits, a plurality of first terminal ~~pad connecting to~~ pads, each of which is connected to one of the first internal ~~circuit~~ circuits and a plurality of conductive relay [[pad]] pads, each of which is isolated from the first terminal [[pad]] pads, wherein each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second

semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of metal [[bump]] bumps, each of which is formed on one of the conductive relay [[pad]] pads;

a first bonding wire, wherein one end thereof is formed on one of the first terminal [[pad]] pads and the other end is formed on the first conductive pattern;

a second bonding wire, wherein one end thereof is formed on the second conductive pattern and the other end is formed at the top of one of the metal [[bump]] bumps; and

a third bonding wire, wherein one end thereof is formed on the second terminal pad and the other end is formed at the top of the one of the metal [[bump]] bumps;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 18 (cancelled).

Claim 19 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 13, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 20 (currently amended): A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a plurality of first conductive ~~portion~~ portions and a plurality of second conductive ~~portion, the second conductive portion having~~ portions, each of which has a first area and a second area, which is different from the first area, wherein each first conductive portion and each second conductive portion are alternatively aligned;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a third conductive portion, connected to one of the second conductive portion in the first area;

a plurality of [[bump]] bumps, each of which is formed on one of the second conductive [[portion]] portions in the second area;

a first internal terminal connected to one of the first conductive [[portion]] portions;

a second internal terminal connected to one of the second conductive [[portion]] portions in the second area; and

a wire, wherein one end thereof is formed on the second internal terminal and the other end is formed at the top of the one of the [[bump]] bumps.

Claim 21 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are located along a side of the first semiconductor chip.

Claim 22 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating

substrate, and the first semiconductor chip is placed on the insulating substrate.

Claim 23 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 20, wherein the first area and the second area are spaced from each other.

Claims 24-29 (cancelled).

Claim 30 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 1, wherein <u>each of</u> the first terminal [[pad]] <u>pads</u> is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claims 31 (cancelled).

Claim 32 (currently amended): A multi-chip package type semiconductor

device, as claimed in claim 13, wherein each of the first terminal [[pad]] pads is rectangularly-shaped, and a side of the first terminal pad is parallel to a side of the first semiconductor chip.

Claims 33 (cancelled).

Claim 34 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 15, wherein each of the first terminal [[pad]] pads is rectangularly-shaped, and a side of the first terminal pad is parallel to the side of the first semiconductor chip.

Claims 35 (cancelled).

Claim 36 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 20, wherein each of the first conductive ~~portion~~ portions is rectangularly-shaped, and a side of the first conductive portion is

parallel to a side of the first semiconductor chip.

Claim 37 (currently amended): A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a plurality of first internal ~~circuit~~ circuits on the insulating substrate, the first semiconductor chip having a plurality of first terminal ~~pad connecting to~~ pads, each of which is connected to one of the first internal ~~circuit~~ circuits and a plurality of conductive relay [[pad]] pads, each of which is isolated from the first terminal [[pad]] pads, and ~~the conductive relay pad including~~ each of which includes a first area and a second area, which is different from the first area, each first terminal pad and each conductive relay pad are alternatively aligned;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having

a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a plurality of metal [[bump]] bumps, each of which is formed on one of the conductive relay [[pad]] pads in the second area;

a first bonding wire, wherein one end thereof is formed on one of the first terminal [[pad]] pads and the other end is formed on the first conductive pattern;

a second bonding, wherein one end thereof is formed on the second conductive pattern and the other end is formed on one of the conductive relay [[pad]] pads in the first area; and

a third bonding wire, wherein one end thereof is formed on the second terminal pad and the other end is formed at the top of the metal bump on the one of the conductive relay [[pad]] pads in the second area;

wherein the lengths of the first, second and third bonding wire are approximately the same.

Claim 38 (previously presented): A multi-chip package type semiconductor

device, as claimed in claim 37, wherein the second semiconductor chip is placed on the center of the first semiconductor chip

Claim 39 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 38, wherein each of the conductive relay [[pad]] pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a longer side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip, wherein a distance from the side of the first semiconductor chip to the first area is almost the same as that from the side of the first semiconductor chip to the second area.

Claim 40 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 38, wherein each of the conductive relay [[pad]] pads is rectangularly-shaped, and is formed on a periphery of the first semiconductor chip, and a shorter side of the rectangularly-shaped conductive relay pad is parallel to a side of the first semiconductor chip.

Claim 41 (previously presented): A multi-chip package type semiconductor device, as claimed in claim 40, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

Claim 42 (currently amended): A multi-chip package type semiconductor device, as claimed in claim 38, wherein each of the metal [[bump]] bumps is spaced apart from the ~~first bond~~ one end of the second bonding wire, but is electrically connected to the ~~first bond~~ one end of the second bonding wire via the conductive relay pad.